Principles of VLSI RTL Design: A Practical Guide

Von Sanjay Churiwala, Sapan Garg
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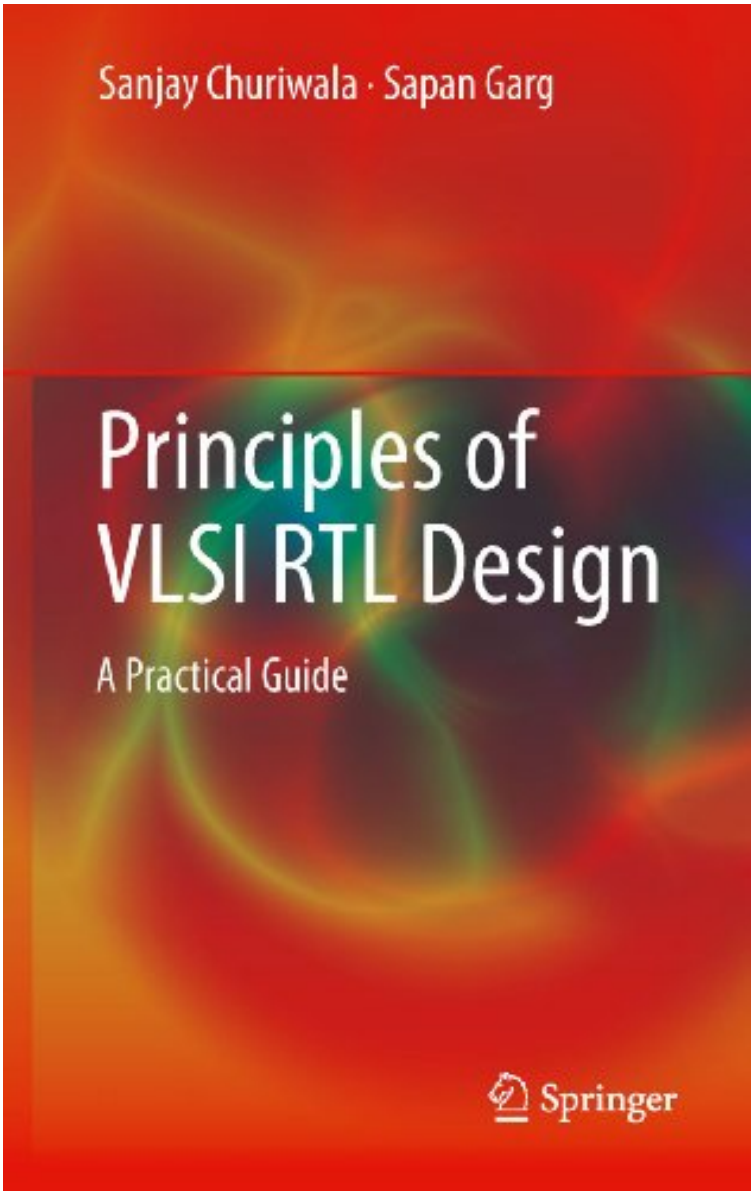

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Von Sanjay Churiwala, Sapan Garg : Principles of VLSI RTL Design: A Practical Guide before purchasing it in order to gage whether or not it would be worth my time, and all praised Principles of VLSI RTL Design: A Practical Guide:

KundenrezensionenHilfreichste Kundenrezensionen0 von 0 Kunden fanden die folgende Rezension hilfreich. Principles of VLSI RTL Design : A Practical GuideVon MiroslavGood focus and organization of the book. Some

useful information for every RTL designer can be found in this book.Clearly, the quantity of such new information strongly depends on designer experience. One should know that many information which this book contains can be found in Synopsys documentation, with more details. For example, the chapters 3 ("Timig Analysis") and 7 ("Timing Exception") can be connected to the Synopsys document : "Timing Constraints and Optimization User Guide". However, the writing style of the book is chatty, which appeals to me.

KurzbeschreibungSince register transfer level (RTL) design is less about being a bright engineer, and more about knowing the downstream implications of your work, this book explains the impact of design decisions taken that may give rise later in the product lifecycle to issues related to testability, data synchronization across clock domains, synthesizability, power consumption, routability, etc., all which are a function of the way the RTL was originally written. Readers will benefit from a highly practical approach to the fundamentals of these topics, and will be given clear guidance regarding necessary safeguards to observe during RTL design.KurzbeschreibungSince register transfer level (RTL) design is less about being a bright engineer, and more about knowing the downstream implications of your work, this book explains the impact of design decisions taken that may give rise later in the product lifecycle to issues related to testability, data synchronization across clock domains, synthesizability, power consumption, routability, etc., all which are a function of the way the RTL was originally written. Readers will benefit from a highly practical approach to the fundamentals of these topics, and will be given clear guidance regarding necessary safeguards to observe during RTL design.BuchrckseiteIn the process of integrated circuit design, front-end activities start with a register transfer level (RTL) description, of the functionality desired from the IC. During subsequent steps in the design flow, issues may arise related to testability, data synchronization across clock domains, synthesizability, power consumption, routability, etc. which are a function of the way the RTL was originally written.As a result, RTL designers need to take care of many aspects which can have impact on later steps in the design process. Since RTL design is less about being a bright engineer, and more about knowing the downstream implications of your work, this book explains those various aspects, their significance, what caution needs to be taken during RTL design and why. Readers will benefit from a highly practical approach to the fundamentals of uncertainties around functionality, clock domain crossing and clock synchronization, design for test and testability, power consumption, static timing analysis, timing exception handling, and routing congestion.Hopefully, this book will find its place in the hearts and minds of anyone whogenerates RTL code. This includes RTL designers as well as those writing toolsthat generate RTL. Relatively new RTL designers will find this book to be a single-source of interesting, rich and useful knowledge. Experienced RTL designers will be able to appreciate and cement some already known concepts, given the focus on practical situations encountered in real designs.* Provides a highly accessible, single-source reference to all key topics essential to an RTL designer; * Describes in detail specific actions/cautions that designer needs to consider in design to avoid problems in downstream implementation;* Covers content based on practical experience with numerous real designs from large semiconductor design companies.